THRESHOLD VOLTAGE INSTABILITY IN A-SI:H TFTS AND THE IMPLICATIONS FOR FLEXIBLE DISPLAYS AND CIRCUITS

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ABSTRACT

After a brief review of the characteristics of electrical stress degradation of flexible, amorphous silicon thin film transistors, the implications for various types of flexible circuitry including active matrix backplanes, integrated drivers and general purpose digital circuitry are examined. A circuit modeling tool that enables the prediction of complex circuit degradation is presented. Experimental results for a variety of flexible digital circuits including programmable logic arrays and memories are presented. Finally, we discuss the principal remaining challenges to building a fully flexible electronic system.

1. INTRODUCTION

There is current interest in extending amorphous silicon (a-Si:H) thin film transistor (TFT) technology to flexible substrates [Long, et al., 2006, O'Rourke, et al., 2008] for lightweight, rugged displays conformal to shaped surfaces (Fig. 1). Eventually, wearable, flexible displays integrated into clothing will be useful in applications such as providing real time situational awareness for soldiers and emergency personnel. The application of flexible electronics beyond displays has already begun with the integration of a-Si:H row and column drivers and general purpose a-Si:H digital logic such as programmable logic arrays [Stewart and Lebrun, 1997, Venugopal and Allee, 2007, Shringarpure, et al., 2008a] (Fig. 2). Ultimately, one can envisage fully flexible systems including sensors, microcontroller, display and flexible power sources, enabling applications such as a 'smart' medical bandage capable of sensing and displaying patient information and vital signs.

In this paper, we review the progress and challenges in flexible a-Si:H electronics at the Flexible Display Center. In section 2, our a-Si:H thin film transistor structure and characteristics are reviewed. In section 3, electrical stress induced degradation of a-Si:H TFTs is reviewed followed by measurements and discussion of the impact on various type of flexible circuits in section 4. Finally in section 5, we discuss the remaining challenges in implementing a fully flexible electronic system.

3. A-SI:H THIN FILM TRANSISTORS

The a-Si:H TFT developed at the Flexible Display Center is a bottom gate inverted staggered structure fabricated with a low temperature (180°C) process compatible with flexible substrates, e.g., stainless steel and heat stabilized polyethylene naphthalate [O'Rourke, et al., 2008]. The gate dielectric is silicon nitride. There are three metal layers in this process. The saturation mobility is 0.8 cm^2/Vs with an on/off current ratio greater than 10^8. The subthreshold slope is approximately 0.6 V/decade. The threshold voltage is slightly greater than 1 V after fabrication (Fig. 3). The hysteresis between forward and reverse sweeps of the drain-source voltage is also approximately 1V.

Fig. 1: An active matrix QVGA electrophoretic display fabricated on flexible stainless steel.

Fig. 2: Flexible electronics on flexible plastic (PEN, left) and stainless steel (right) substrates

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14. ABSTRACT

15. SUBJECT TERMS

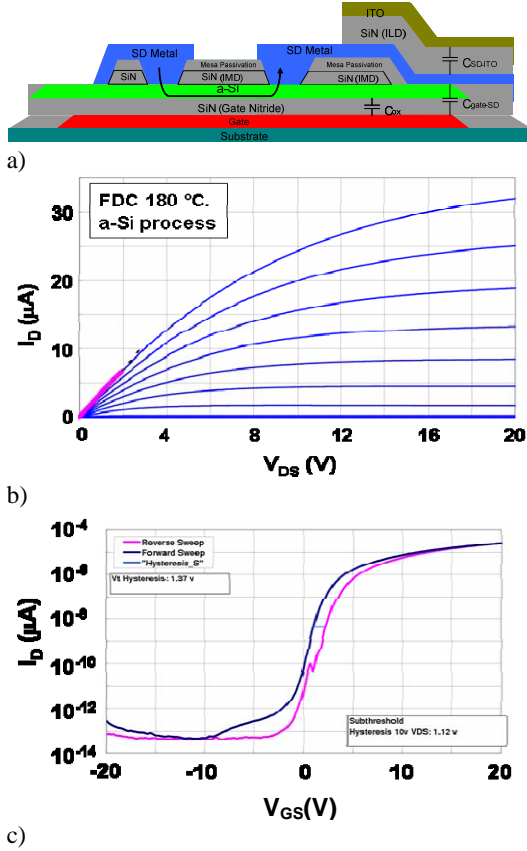| 16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
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Fig. 3. a) A cross section of the low temperature a-Si:H TFT process developed at the Flexible Display Center. b) Typical I-V characteristics of an a-Si:H TFT: I_d vs V_{ds} on a linear scale with V_{gs} as a parameter, and c) I_d vs V_{gs} on a log scale showing the subthreshold slope and reverse leakage current.

2. THRESHOLD VOLTAGE INSTABILITY

A primary consideration in circuit design with a-Si:H thin film transistors is that they are unstable electrically, primarily due to an electric field induced threshold voltage (V_{th}) shift [Chiang, et al., 1998]. This gradual increase in V_{th} limits the lifetime of active matrix backplanes and is more severe on low temperature processes required for flexible backplanes [Gleskova and Wagner, 2001]. Fig. 4 shows the measured V_{th} shift (ΔV_{th}) on some of our prototype devices. Furthermore, ΔV_{th} is a strong function of aggregate time a transistor is biased on, accentuating the increase in threshold voltage for general purpose digital circuitry where, unlike the TFTs in a display backplane, the transistors operate continuously.

The two mechanisms responsible for the ΔV_{th} in a-Si:H TFTs are charge injection in the silicon nitride (SiN_x) gate insulator and creation of defect states in the a-Si:H conducting channel [Powell, 1989]. Field-effect experiments have provided evidence that mobile carriers are responsible for breaking the weak Si–H

bonds resulting in the creation of charged defect states (dangling bonds).
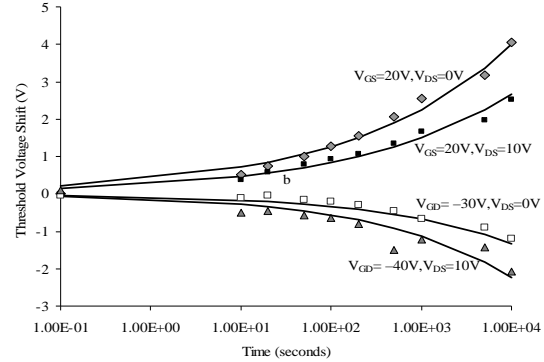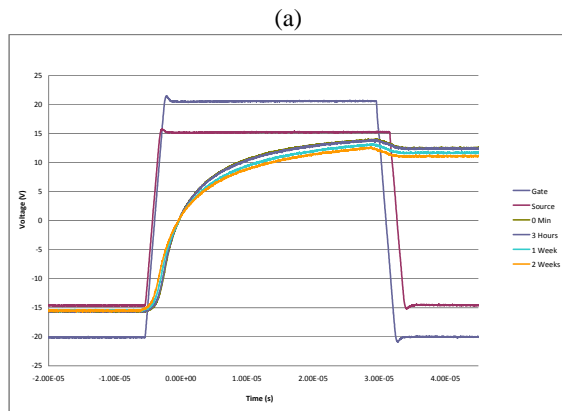

Fig. 4. Threshold voltage shift vs. time for positive and negative gate voltages with and without elevated drain voltages for FDC TFTs.

Extending techniques used to localize hot electron degradation in MOSFETs, experiments in our lab have localized the degradation of a-Si:H to the gate dielectric/a-Si:H channel interface [Shringarpure, et al., 2008b]. The TFTs were subjected to gate bias stress in the linear and saturation modes, and the drain source current was measured in the forward (drain and source the same as during the application of stress) and reverse (source and drain interchanged) configurations. For gate bias stress in saturation, increased drain source current measured with the source and drain reversed indicates localization of ΔV_{th} to the gate dielectric/amorphous silicon interface.
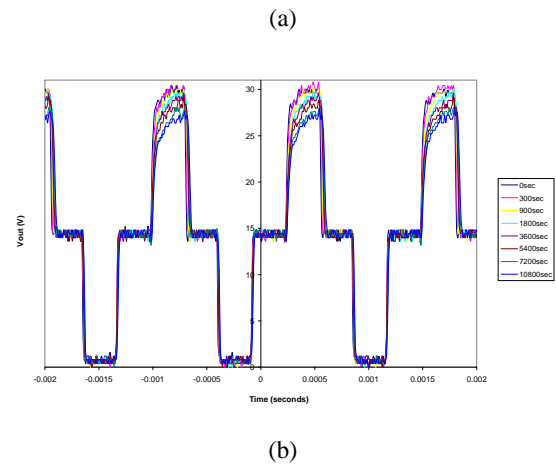
Further experiments in our lab on a-Si:H thin film transistors demonstrated ΔV_{th} recovery of several volts after room temperature rest with no applied voltage (supplies floating) [Venugopal, et al., 2006]. Inverters and 10 transistor latch circuits were stressed with a 50% duty cycle input and rested at room temperature without any applied voltage. Substantial recovery of the threshold voltages was observed. However, subsequent electrical stress rapidly degraded the threshold voltage to the pre-rest value. Hence, the threshold voltage recovery observed in a-Si:H circuits after periods of rest is temporary, and cannot be used to extend the total operational circuit lifetime. This response is similar to that observed with negative bias stress instability in bulk CMOS circuits, which may indicate similar physical mechanisms.

3. IMPACT ON CIRCUIT PERFORMANCE

In spite of the rapid V_{th} increase with positive gate voltages, long lifetimes are possible in active matrix backplanes since each transistor in the backplane is only on, i.e., its channel occupied by carriers, when the row it is in is activated. The duty cycle of an individual transistor is one out of N rows. For a QVGA display,

there are 240 rows and 320 columns. Each transistor in the backplane has a duty cycle of 0.4% resulting in a small average gate voltage. Since the time dependence of the rise in threshold voltage is sub-unity (~0.3), dramatically increased lifetimes are possible for active matrix backplanes. Some displays apply a negative V_{GS} when the row is off, achieving further reduction in threshold voltage shift by allowing some recovery during the off time.

(a)

(b)

Fig. 5. (a) Pixel circuit including parasitics for electrophoretic display and, (b) Measured voltage at storage node initially and after 3 hr, 1 week and 2 weeks of continuous operation.

Electrical stress degradation measurements were made on an active matrix backplane pixel for electrophoretic QVGA displays (Fig. 5). The pixel TFT is turned on with a +20 V gate voltage allowing the data on the source line to be stored on the storage capacitor. The TFT is on for one row time and off for the remainder of the frame which is ~16 ms for a 60 Hz frame rate. The off gate line voltage is -20 V. For this experiment, the source line data alternated between plus and minus 15 V corresponding to black and white states of the pixel. As can be seen in Fig. 5(b), there is negligible degradation of the stored pixel voltage after 2

weeks of continuous operation even for our low temperature a-Si:H TFT process. For higher temperature a-Si:H processes typical of glass active matrix backplanes for LCDs, TFT lifetimes have been measured to be more than 10,000 hours at 70°C [Chiang, et al., 1998].

(a)

(b)

Fig. 6. (a) Schematic of integrated a-Si:H column driver for an electrophoretic display, and (b) Measured sequential column voltages of 30 V, 15 V and 0 V after various periods of time of continuous operation. Note that the 30 V output has degraded to ~27 V after 10,000 seconds.

Integrated column drivers are more challenging since they must be continuously active to provide data to the columns during every row access. This implies a large duty cycle and shorter lifetimes before the V_{th} rises to unacceptable levels. We have developed integrated a-Si:H column drivers for flexible, electrophoretic displays [Venugopal and Allee, 2007] in order to reduce the number of column interconnects off the flexible backplane, improving both reliability and cost. A high speed shift register to bring the column data in on a single interconnect is not achievable with the low mobility and slow speed of a-Si:H circuitry. Consequently, the design we developed uses parallel shift registers to achieve the necessary bandwidth. The compromise architecture reduces the number of column interconnects from the display to the controlling board by over 3x. The circuitry for a single column (Fig. 6(a)) is composed of a series of dynamic latches and inverters that translate 2 bits of digital information into one of the three column voltages.

This integrated a-Si:H column driver was operated continuously at typical display speeds driving 30 V, 15 V and 0 V sequentially onto a column (see Fig. 6(b)). Due to electrical stress degradation of the final TFTs driving the column voltages, the 30 V column signal rapidly decreases. After 10,800 seconds, the highest column voltage has decreased 10%.

Therefore, amorphous silicon column drivers are not suited for continuous motion video display operation, but are for applications with occasional image updates. Such applications include commercial signage, smart card displays, electronic maps, and smart medical bandages. For example, flexible, lightweight, robust bandages could incorporate sensors and an a-Si:H microcontroller that are powered down most of the time. Once every few minutes, the circuitry would awaken, take a measurement, perform simple calculations, display the result on an integrated, bistable flexible display and return to sleep mode. Both of these applications can successfully utilize flexible, digital a-Si:H circuits and have product lifetimes of months or years. For this column driver design and our low temperature a-Si:H process, we estimate that over $2x10^4$ image updates every half second are possible before the threshold voltage rises by 20%, where the circuit will still be fully operational.

To demonstrate general digital logic on flexible a-Si:H, we fabricated both static and dynamic programmable logic arrays (PLA) of flexible stainless steel [Shringarpure, et al., 2008a]. The absence of a p-type device in a-Si:H technology makes programmable logic arrays attractive since they minimize the number of pull-up devices. The pull-up loads are diode connected n-type a-Si:H TFTs. Both the static and dynamic arrays use high fan-in NOR gates for the AND and OR planes. Both arrays have 12 inputs, 24 outputs, up to 35 minterms and implement the instruction decoder for a flexible microcontroller. The output buffers are bootstrapped gates providing a full V_{DD} logic high level.

The static PLA has the advantage of timing simplicity but with increased power consumption, slower speed and poor noise margins. Measurements indicated correct instruction decode operation for the static PLA fabricated on flexible stainless steel. The propagation delay was 105 µs driving a 20pF load capacitor. The average power consumption was 8.7 mW (V_{DD} = 25 V) primarily due to the heavy load capacitance.

The dynamic PLA reduces power consumption, increases speed and improves noise margin but at the expense of complicated clocking. A portion of the schematic of the dynamic PLA is shown in Fig. 7 along with the layout. The dynamic design incorporates a 4

phase clock with two additional complementary clocks. The clocks gate the pull-up transistors and the footed NOR arrays limiting the static power consumption. Importantly, this clocking scheme avoids the critical timing race typical of conventional CMOS dynamic PLAs. The dynamic PLA on flexible stainless steel was fully functional with a propagation delay of 36 µs and an average power consumption of 3.5mW. Again, most of this power consumption was consumed driving the large load capacitances.
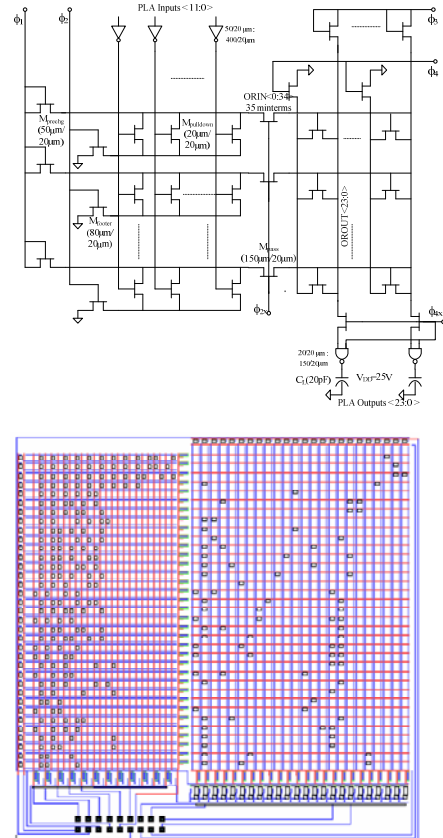

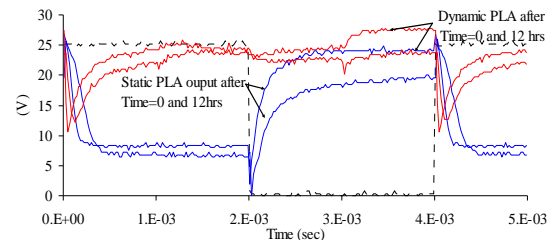Fig. 7. The a-Si:H dynamic programmable logic array.

Fig. 8. Measured static and dynamic PLA outputs after 12 hrs of continuous operation.

Finally, the dynamic programmable logic array withstands electrical stress better than the static design. In figure 8, two outputs from the static and dynamic PLAs are plotted both for the initial response and after 12 hours of continuous operation. The dynamic PLA has better output high voltages both before and after electrical stress.

We have also recently fabricated an array of static random access memory (SRAM) cells in the low temperature, a-Si:H process. The architecture is the typical fully differential CMOS SRAM 6 transistor cell with the two p-type devices replaced with diode connected n-type a-Si:H TFTs (Fig. 9). A write operation is implemented by asserting a word line and connecting the bit lines to data and data bar thereby loading the bits into the back to back inverters. A read is accomplished by precharging the bit lines high and asserting the desired word line. The selected cells either pull a bit line low indicating a 0 or leave the bit line high indicating a 1. The functionality of the SRAM array writing and reading 1 and 0 was experimentally verified (Fig. 10). Further tests on the number of reads and writes possible before electrically stress wears out the cell are underway.
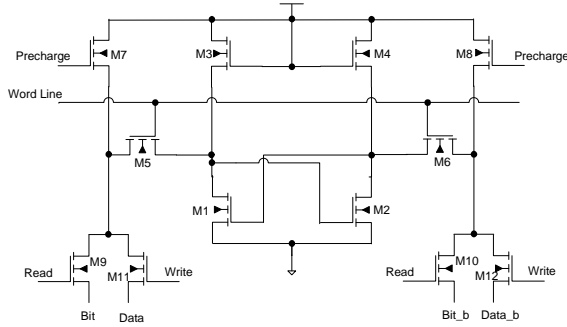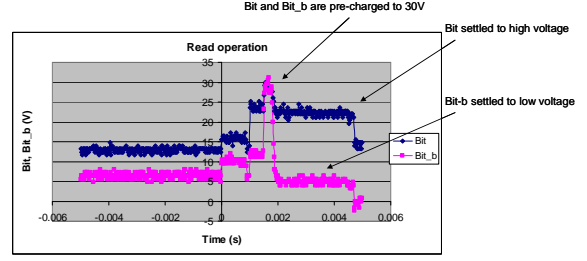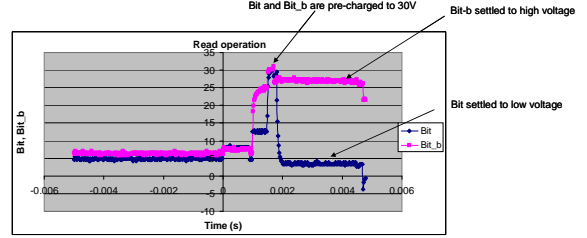

Fig. 9. Schematic of the a-Si:H TFT SRAM. M1-M6 form the repeating cell in the array. M7-M12 occur only once per column.

4. CIRCUIT SIMULATOR TO PREDICT AGING

In a-Si:H circuits, each device experiences a different average gate voltage and hence degrades at a different rate. It is important to have a circuit simulator that can predict the complex post-degradation response of arbitrary a-Si:H TFT circuits. To this end, we have developed a computer model of the ΔV_{th} and incorporated that model in SPICE circuit simulator [Shringarpure, et al., 2007]. The V_{th} degradation model is added to the Spice 3.0 TFT device model to obtain a composite model and is verified by comparing the simulated V_{th} shift with measured data in a TFT latch circuit.

Fig. 10. Experimental measurements of a-Si:H TFT static random access memory cell. a) Correct reading of a stored 1. b) Correct reading of a stored 0.

The ΔV_{th} can be given by

$$\Delta V_{th}(t) = A \cdot exp\left(-\frac{E_A}{kT}\right) \cdot t^\beta \left(V_{GS} - \eta V_{DS} - V_{th,0}\right)^n.$$

(1)

where k is the Boltzmann constant, T is the absolute temperature, and t is the bias stress time duration. E_A is the mean activation energy of the transistor aging process with A being the degradation rate. β and n are process related constants. Due to the non-linear nature of (1), an intermediate parameter Age, which is a linear function of the stress time is introduced. The Age parameter provides the means to quantify the degradation suffered by individual TFTs in the circuit and is related to (1) by

$$\Delta Age(\Delta t_i) = \int_{t_{i-1}}^{t_i} A^{1/\beta} \cdot exp\left(-\frac{E_A}{\beta KT}\right) \cdot \left(V_{GS} - \eta V_{DS} - V_{t,0}\right)^{n/\beta} dt \quad (2)$$

where V_{GS} and V_{DS} are the biases during the simulation time-step $\Delta t_i = t_i - t_{i-1}$. The incremental Age's (ΔAge) are summed to obtain the total Age at the end of the simulation time (t_{stop}) after which the total Age (i.e. Age(t_{stop})) is extrapolated to a user specified post-stress circuit age (t_{age}), to give the net ΔV_{th} experienced by the a-Si:H TFT. The ΔV_{th} model assumes that the stimulus applied for the simulation period to obtain the total Age can be approximated by a periodic application of the stimulus used in (2) to give the extrapolated ΔV_{th}, i.e., a periodic stimulus is assumed. The ΔV_{th} model has been added to the RPI Level-15 ATFT model and to the BSIM3 model, which we have found can fit our a-Si:H TFTs very well, where the combined models are incorporated into the NG-Spice (Spice 3.0) circuit

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simulator. The model accurately predicts the actual measured circuit responses with circuit aging over several hours as previously reported [Shringarpure, et al., 2007], and work is underway to improve the accuracy for extended durations of electrical stress.
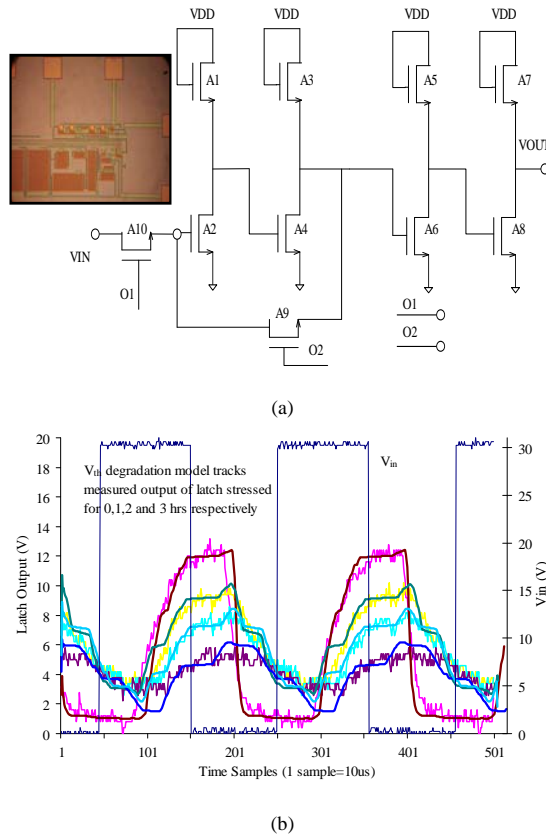

(a)

(b)

Fig. 11. (a) Latch circuit using n-type TFTs and a latch photo (inset), (b) Simulated and measured latch outputs without stress and after applying stress for 1, 2, and 3 hours, respectively.

5. PATH TO FULLY FLEXIBLE SYSTEM

The ultimate goal is a fully flexible electronic system incorporating display, drivers, digital logic, sensors and analog sensor interface, antennas, radio frequency transmit / receive circuitry, and finally a flexible power supply. Such a system would have DoD applications such as smart medical bandages, blast dosimeters, tagging and tracking, and unattended ground sensors. It is instructive to consider what flexible TFT technology can currently achieve and what challenges remain. Before we begin, it should be noted that it is possible to build flexible, high performance single crystal silicon integrated circuits by removing the backside of a silicon wafer through grinding or other means (www.semprius.com). Here, we focus on larger area, lower cost thin film transistor technology.

Beginning with the components already

demonstrated, flexible active matrix reflective displays were developed by DARPA in the 1990s [Wu, et al., 1997] and are currently being manufactured in small volume. Integrated a-Si:H row drivers have been incorporated in commercial displays and are readily transferable to flexible technology. Both of these components will have substantial lifetime in spite of the electrical stress degradation of a-Si:H.

Complex digital logic has been demonstrated in flexible a-Si:H as reviewed in this paper. This category includes integrated column drivers for displays, programmable logic arrays and memories. With these components, a complete microcontroller is achievable. However, electrical stress degradation of a-Si:H does limit the lifetime for digital circuits to roughly a billion clock cycles. This is only 2 weeks of operation at kHz clocking speeds typical of a-Si:H TFTs. However, it may be suitable for applications that are powered down most of the time and occasionally awaken to sense, calculate and display some information. Since amorphous silicon is a mature technology, it is unlikely that a breakthrough will completely solve the electrical stress degradation issues. However, other thin film transistor materials are emerging – ZnO, nc-Si, various nanowire and organic TFTs – and their stability has not been fully explored. Nano-crystalline silicon appears particularly promising in this regard [Lee, et al., 2007].

Flexible antennas appear quite doable. Projects are currently underway in our lab to fabricate a GHz bow tie antenna on plastic complete with matching network and baluns. Some electroplating may be necessary to reduce the resistance of the deposited metal layers. In addition, we are working on flexible frequency selective surfaces fabricated on plastic.

Sensors are also readily fabricated on flexible substrates. An electrochemical sensor fabricated on PEN has demonstrated 20 ppm sensitivity for explosives (TNT) (Prof. Joseph Wang, UC San Diego, private communication). We are currently fabricating a flexible MEMs capacitive sensor for the detection of shock waves and blast dosimetry.

Flexible batteries and flexible solar cells are already commercially available (for example, www.bluesparktechnologies.com and www.siliconsolar.com).

Transmit and receive circuitry pose a difficult challenge. For a near earth transmitter, transmit frequencies need to be at least VHF for appreciable energy to be radiated as opposed to being dissipated in the earth. This will require carrier mobility on the order of 100 cm^2/Vs whereas a-Si:H TFTs have a carrier mobility of 1 cm^2/Vs. Clearly, a higher mobility material is needed. However, none of the candidate materials currently being studied have demonstrated the required mobility in a repeatable, manufacturing environment with the possible exception of laser

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recrystallized polycrystalline silicon [Howell, et al., 2000].

Alternate transmit and receive architectures may be needed to circumvent the traditional high speed and high mobility transistors. Reception can be minimally achieved with a single high speed diode, and an organic diode has been reported with 50 MHz operation [Steudal, et al., 2005]. Transmission might be possible with a programmable, frequency selective surface functioning as a passive radar reflector. Possibly, an infrared link might be built in ZnO, a direct bandgap semiconductor.

A second major challenge is the absence of a flexible operational amplifier for analog sensor interface electronics. The op-amp does not necessarily have to have high speed, but must have high gain and preferably stability. High gain requires a high impedance load device and a consequent gain per stage of at least 20. Resistors as load devices for a-Si:H TFTs are impractically large. P-type a-Si:H devices have very low carrier mobility. A diode connected a-Si:H load device results in a gain per stage of only 2 to 3. As a result, our efforts to fabricate a flexible, a-Si:H only, operational amplifier have been unsuccessful.

A possible solution for a flexible operational amplifier is to incorporate p-type organic TFTs with n-type a-Si:H TFTs forming low power, flexible CMOS. Such a combination has been achieved for rigid digital circuits [Bonse, et al., 1998], and we have been developing a flexible CMOS process in collaboration with the University of Texas at Dallas. Experimental results for flexible digital CMOS circuits will be presented at an upcoming conference on flexible electronics and displays. The integration of p-type organic load devices with a-Si:H technology may also enable flexible operational amplifiers. A potential remaining challenge is electrical stability. Operational amplifiers require matched transistors for proper operation, and the drift of TFT electrical parameters with electrical stress will make matching problematic. However, residual small offsets due to mismatches have long been removed from CMOS op-amps with circuit techniques such as correlated double sampling. The extent to which these specialized circuits can remove much larger offsets in flexible CMOS op-amps is yet to be determined.

6. CONCLUSIONS

We have reviewed the electrical stress degradation characteristics of a-Si:H thin film transistors and studied their impact on various types of circuits including displays, integrated display drivers, complex digital logic and memories. Computer aided design tools have been developed to predict the aging of arbitrary a-Si:H circuits where each device experiences different voltages and hence different aging. Finally, the achievable components and remaining challenges of a fully flexible electronic system including display, logic, sensors/sensor interface, power and communication link were discussed.

5. References

Bonse, M.; Thomasson, D.B.; Klauk, H.; Gundlach, D.J.; Jackson, T.N., 1998 : Integrated a-Si:H/pentacene inorganic/organic complementary circuits, Technical Digest of International Electron Devices Meeting, 1998, pp. 249-252

Chiang, C.; Kanicki, J.; and Takechi, K., 1998: Electrical instability of hydrogenated amorphous silicon thin-film transistors for active matrix liquid crystal displays, *Japanese Journal of Applied Physics*, **37**, pp. 4704-4710

Gleskova, H.; and Wagner, S., 2001: DC-gate-bias stressing of a-Si:H TFTs fabricated at 150C on polyimide foil, *IEEE Transactions on Electron Devices*, **48**, pp. 1667-1671

Howell, R.S.; Stewart, M.; Kamik, S.V.; Saha, S.K.; Hatalis, M.K., 2000: Poly-Si thin-film transistors on steel substrates, *IEEE Electron Device Letters*, **21**, pp. 70 - 72

Lee, C.H.; Striakhilev, D.; Nathan, A., 2007: Stability of nc-Si:H TFTs With Silicon Nitride Gate Dielectric, *IEEE Trans. On Electron Devices*, **54**, pp. 45- 51

Long, K.; Kattamis, A.Z.; Cheng, I.C.; Gleskova, H.; Wagner, S.; and Sturm, J.C., 2006: Stability of amorphous-silicon TFTs deposited on clear plastic substrates at 250C to 280C, *IEEE Electron Device Letters*, **27**, pp. 111-113

O'Rourke, S.M.; Venugopal, S.M.; Raupp, G.B.; Allee, D.R.; Ageno, S.; Bawolek, E.J.; Loy, D.E.; Kaminski, J.P.; Moyer, C.; O'Brien, B.; Long, K.; Marrs, M.; Bottesch, D.; Dailey, J.; Trujillo, J.; Cordova, R.; & Toy, D., 2008: Active Matrix Electrophoretic Displays on Temporary Bonded Stainless Steel Substrates with 180 °C a-Si:H TFTs, *Society for Information Display, International Symposium digest of technical papers*, 2008.

Powell, M.J., 1989: The physics of amorphous-silicon thin-film transistors, *IEEE Trans. Electron Devices*, **36**, pp. 2753-2763

Stewart, R.; Lebrun, H., 1997: Reliability and lifetime of SASID Displays, *International Displays Workshop*, Nagoya, Japan, Nov 1997.

Shringarpure, R.; Venugopal, S.; Li, Z.; Clark, L.T.; Allee, D.R.; Bawolek, E.; and Toy, D., 2007: Circuit Simulation of Threshold Voltage Degradation in a-Si:H TFT's Fabricated at 175°C, *IEEE Transactions on Electron Devices,* **54**, pp. 1781-1783

Shringarpure, R.; Clark, L.T.; Venugopal, S.M.; Allee, D.R.; and Uppili, S.G., 2008: Amorphous Silicon Logic Circuits on Flexible Substrates, *Proceedings of 2008 IEEE Custom Integrated Circuits Conference*, Sept. 21-24, 2008, San Jose, California

Shringarpure, R.; Venugopal, S.; Clark, L.T.; Allee, D.R.; Bawolek, E., 2008: Localization of gate biased induced threshold voltage degradation in a-Si:H TFTs, *IEEE Electron Device Letters, 29*, pp. 93-95

Steudel, S.; Myny, K.; Arkhipov, V.; Deibel, C.; De Vusser, S.; Genoe, J.; and Heremans, P., 2005: 50 MHz rectifier based on an organic diode, *Nature Materials* **4**, pp. 597 - 600

Venugopal, S.M.; Allee, D.R.; Li, Z.; and Clark, L.T., 2006: Threshold-voltage recovery of a-Si:H digital circuits, *Journal of the Society for Information Displays*, **14**, pp. 1053-1057

Venugopal, S.M. and Allee, D.R., 2007: Integrated a-Si:H source drivers for 4 QVGA electrophoretic display on flexible stainless steel substrate, *IEEE Journal of Display Technology*, **3**, pp. 57-63

Wu, C.C.; Theiuss, S.D.; Gu, G.; Lu, M.H.; Sturm, J.C.; Wagner, S.; Forrest, S.R., 1997: Integration of organic LEDs and amorphous Si TFTs onto flexible and lightweight metal foil substrates, *IEEE Electron Device Letters*, **18**, pp. 609-612